

Remarks

I. Status of claims

Claims 1-38 are pending.

II. Claim objections

The Examiner has objected to the claims because “the transitional term ‘comprising’ should be followed by a colon to clearly differentiate between the preamble of the claimed invention and the body of limitations.”

In claim 1, a colon has been added to the preamble and the structure of the claim body has been modified to address the Examiner’s concerns.

The remaining claims are believed to be sufficiently precise, clear, correct and unambiguous that no additional punctuation is required.

III. Non-statutory double patenting rejection

The Examiner has provisionally rejected claims 1-38 under the doctrine of obviousness-type of double patenting over claims 1-21 of copending U.S. Patent Application No. 09/971,135, which is commonly owned with the present application by Hewlett-Packard Development Company, L.P. The Terminal Disclaimer being filed herewith should overcome this obviousness-type double patenting rejection.

IV. Claim rejections under 35 U.S.C. § 102(e)

A. Claims 1, 8, 13-14, 16, 18-21, 23-27, 31, 33, and 35-38

The Examiner has rejected claims 1, 8, 13-14, 16, 18-21, 23-27, 31, 33, and 35-38 under 35 U.S.C. § 102(e) over Morioka (U.S. 6,631,447).

1. Independent claims 1, 24, and 38

The Examiner has asserted that:

Morioka teaches the invention (claims 1, 24, and 38) including a multi-computer system, comprising a plurality of local nodes interconnected by a shared memory, each local node comprising:

a local processor (e.g., see Figure 1);

a local memory (e.g., see Figure 1);

a local communications protocol stack as network protocol (e.g., see col. 8, line 31 to col. 9, line 7); and

a shared memory interface system operable to provide a local shared memory network between the local nodes, and a global shared memory network between the local nodes and one or more remote nodes by capturing packets from the local communications protocol stacks and routing the captured packets over the shared memory (e.g., see Figures 15-16 and col. 20, line 21 to col. 24, line 24).

Contrary to the Examiner's assertion, however, each of the local nodes in Morioka's multiprocessor system does not include a shared memory interface system that is operable to provide a local shared memory network between the local nodes, and a global shared memory network between the local nodes and one or more remote nodes by capturing packets from the local communications protocol stacks and routing the captured packets over the shared memory.

With respect to the second embodiment, which is cited by the Examiner, each multiprocessor cluster 100 includes a respective cluster communication unit 500 that "controls inter-cluster communications between respective clusters 100" (col. 22, lines 8-9). Morioka explains that (col. 20, line 66, through col. 21, line 3):

... if the access from the processor 200 is to a local memory 400 in a remote cluster, the cluster communication control unit 500 identifies this, and then transfers the access request via the inter-cluster bus 2200 to a cluster communication unit 500 in the remote cluster.

That is, the access requests between clusters are routed between the cluster communication units 500 over the inter-cluster bus 2200, not over a shared memory that

interconnects the clusters. Indeed, in the second embodiment shown in FIG. 15, the clusters 100 are not interconnected by a shared memory.

With respect to the first embodiment of FIG. 1, each multi-processor cluster 10 includes a respective processor memory interface unit (PMU) 300 that controls processor accesses to local shared memory. Morioka explains that (col. 9, lines 15-19):

When the access request from the processor 200 is to a local shared memory 400 in another cluster remote from therefrom, the access request is transferred to the associated processor memory interface 300 in the remote cluster via the processor global bus 1800.

That is, in the first embodiment, the access requests between the clusters 100 are routed between processor memory interface units 300 over the processor global bus 1800, not the global shared memory 600. Consequently, in the first embodiment, packets from the local communications protocol stacks are not captured and routed over a shared memory that interconnects the clusters 100.

For at least these reasons, the Examiner's rejection of independent claims 1, 24, and 38 under 35 U.S.C. § 102(e) over Morioka should be withdrawn.

2. Dependent claims 8, 13-14, 16, 18-21, 23-27, 31, 33, and 35-38

Claims 8, 13-14, 16, 18-21, and 23 incorporate the features of independent claim 1 and claims 25-27, 31, 33, and 35-38 incorporate the features of independent claim 24. Therefore, claims 8, 13-14, 16, 18-21, 23-27, 31, 33, and 35-38 are patentable over Morioka for at least the same reasons explained above. Each of the claims discussed below also is patentable for the following additional reasons.

a. Claims 8 and 35-37

With regard to claims 8 and 35-37, the Examiner has asserted that "Morioka teaches one or more local nodes comprise one or more physical adapters for connection to one or more remote nodes as part of the overall network configuration such as a NUMA network, a DASH network or a network using SCI protocol (e.g., see col. 1, line 10 to col. 4, line 39).

Claim 8 recites: “one or more local nodes comprise one or more physical network adapters for connection to one or more remote nodes.” Contrary to the Examiner’s assertion, Morioka does not teach that one or more of the clusters 100 include a network adapter for connection to one or more remote nodes. Rather, a network control unit 800, which is not incorporated within any of the clusters 100, controls data transfer between the multi-processor systems and remote nodes in each of the first and second embodiments (see, e.g., col. 8, lines 59-62, and FIGS. 1 and 15).

Claim 35 recites that “the computer program comprises computer-readable instructions for causing a computer to allocate a transmit/receive ring structure in shared memory for each of the other local nodes.” The Examiner’s unfounded assertion regarding one or more local nodes comprising one or more physical adapters does not anticipate the feature recited in claim 35 relating to the allocation of a transmit/receive ring structure in shared memory for each of the other local nodes.

Each of claims 36 and 37 incorporates the features of claim 35 and therefore is patentable over Morioka for at least the same reasons.

b. Claims 13 and 14

Claim 13 recites that “the shared memory interface system on each local node supports multicast and broadcast transmissions over the shared memory for the local shared memory network and the global shared memory network.” The Examiner has asserted that Morioka teaches this feature on col. 27, line 55, through col. 8, line 28.

As explained above in connection with claim 1, the access requests between the clusters 100 are not routed over a shared memory. Instead, in the first embodiment, the inter-cluster access requests are routed between processor memory interface units 300 over the processor global bus 1800 and, in the second embodiment, the inter-cluster access requests are routed between cluster communication control units 500 over the cluster bus 2200. Therefore, neither the processor memory interface units 300 in the first embodiment nor the cluster communication control units 500 in the second embodiment supports multicast and broadcast transmissions over a shared memory interconnecting the local nodes for the local shared memory network and the global shared memory network.

Claim 14 incorporates the features of claim 13 and therefore is patentable over Morioka for at least the same reasons.

Claim 14 also recites that “a broadcast ring structure and a multicast ring structure are allocated in shared memory for each of the local and global shared memory networks.” Morioka does not teach or suggest anything about allocating a broadcast ring structure and a multicast ring structure in a shared memory interconnecting the local nodes. Indeed, in Morioka’s embodiments shared memory is not used as the physical transport medium for network communications.

c. Claims 16 and 18-20

Claim 16 recites that “for each of the local and global shared memory networks a pair of transmit/receive ring structures are allocated in shared memory for each pair of local nodes.” Morioka does not teach or suggest anything about allocating transmit/receive ring structures in a shared memory interconnecting the local nodes. Indeed, in Morioka’s embodiments, shared memory is not used as the physical transport medium for network communications.

Each of claims 18-20 incorporates the features of claim 16 and therefore is patentable over Morioka for at least the same reasons.

d. Claim 21

Claim 21 incorporates the features of claim 16 and therefore is patentable over Morioka for at least the same reasons.

Claim 21 also recites that “a read pointer and a write pointer are associated with each transmit/receive ring structure.” The Examiner has asserted that “Morioka teaches having a read pointer and a write pointer associated with the ring structure as being part of the memory subsystems (e.g., see Figure 16).” FIG. 16, however, does not show a transmit/receive ring structure, much less a read pointer and a write pointer associated with a transmit/receive ring structure. As explained above, Morioka’s embodiments do not use shared memory as the physical transport medium for network communications.

B. Claims 2-7, 9-12, 15, 17, 22, 28-30, 32 and 34

Claims 2-7, 9-12, 15, 17, and 22 incorporate the features of independent claim 1 and claims 28-30, 32, and 34 incorporate the features of independent claim 24. Therefore, claims 2-7, 9-12, 15, 17, 22, 28-30, 32 and 34 are patentable over Morioka for at least the same reasons explained above.

In addition, the sum total of the Examiner's remarks concerning claims 2-7, 9-12, 15, 17, 22, 28-30, 32 and 34 are as follows:

Claims 2-7, 9-12, 15, 17, 22, 28-30, 32 and 34 are considered to read over the art of record.

With this rejection, the Examiner clearly has failed to meet her obligation to consider separately the limitations of each of the pending claims. Indeed, the Examiner is obligated to point to some teaching in the art of record or in the knowledge generally available that anticipates ("read over") all of the features of each of the claims 2-7, 9-12, 15, 17, 22, 28-30, 32 and 34. The Examiner's unsupported and conclusory assertion that these claims "read over the art of record" is insufficient.

In order to establish a proper *prima facie* case of anticipation, the Examiner is requested to point to specific locations in Morioka's disclosure or in another prior art document of record that support her assertions. Alternatively, if the Examiner is aware of facts within her personal knowledge that provide the requisite factual basis to support her deemed conclusion of anticipation, the Examiner is requested to provide an affidavit in accordance with 37 CFR § 1.104(d)(2). In this regard, the Examiner is reminded that (MPEP § 2131, citing *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)):

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.

For at least these additional reasons, the Examiner's rejection of claims 2-7, 9-12, 15, 17, 22, 28-30, 32 and 34 under 35 U.S.C. § 102(e) over Morioka (or whatever unspecified art of record the Examiner had in mind) should be withdrawn.

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V. Conclusion

For the reasons explained above, all of the pending claims are now in condition for allowance and should be allowed.

Charge any excess fees or apply any credits to Deposit Account No. 08-2025.

Respectfully submitted,



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